connecting the input to one of said buses, inputting data and connecting the output to any of said other buses.

7. (Amended) The computer architecture according to claim 1, wherein, when said processor receives an instruction to delete a specific element within a series of data, insert a specific element into said series of data, or add a specific element to the end of a series of data, said processor performs a table lookup, compares the region of data that it manages itself against the position of said element subject to deletion, insertion or addition, and based on the results of said comparison, updates the content of said table.

8. (Amended) The computer architecture according to claim 1, wherein, in response to a given instruction, said processor converts subscripts for specifying elements within a series of data, and/or executes value conversion for giving a specific modification to elements.